## AMENDMENT

**IN THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

**Claims 1-9 (canceled)**

Claim 10. (currently amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thin ~~thick~~ insulating layer disposed over said first and second trench partially filling said first and second trench and being conformal to said first and second trench;

a gate electrode ~~disposed over said thick insulating layer in said first and second trenches, the gate electrode~~ comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion is embedded inside the first trench and said thin ~~thick~~ insulating layer and said first vertical portion within the first trench completely fills the first trench, the second vertical portion is embedded inside the second trench and said thin ~~thick~~ insulating layer and said second vertical portion within the first trench completely fills the second trench, and the horizontal portion is disposed over the substrate and connects said first and second vertical portions together; and

a first shallow doped region within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second vertical portion of the electrode; and

a first deep source region extending from the first shallow doped region and a second deep drain region extending from the second shallow doped region are disposed in a region within the substrate deeper than the first and second trenches.

Claim 11. (currently amended) The structure according to claim 10, wherein the thin ~~thick~~ insulating layer is formed by thermal oxidation.

Claim 12. (currently amended) The structure according to claim 10, wherein a thickness of the thin ~~thick~~ insulating layer is about 0.1 $\mu$m.

Claim 13. (currently amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thin ~~thick~~ insulating layer disposed over said first and second trench, the thin ~~thick~~ insulating layer being conformal to said first and second trench; and

a gate electrode ~~disposed over said first and second trenches, the gate electrode~~ comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical

portion is embedded inside the first trench and said thin ~~thick~~ insulating layer and said first vertical portion within the first trench completely fills the first trench, the second vertical portion is embedded inside the second trench and said thin ~~thick~~ insulating layer and said second vertical portion within the second trench completely fills the second trench, and the horizontal portion is disposed over the substrate and connects said first and second vertical portions together.

Claim 14. (currently amended) The structure according to claim 13, wherein the thin ~~thick~~ insulating layer is formed by thermal oxidation.

Claim 15. (currently amended) The structure according to claim 13, wherein a thickness of the thin ~~thick~~ insulating layer is about 0.1 $\mu$m.

**Claims 16-18 (canceled)**